19-2492; Rev 1; 8/03

5GHz Low-Noise Amplifier with Shutdown

General Description

The MAX2649 high-linearity, silicon-germanium (SiGe) low-noise amplifier (LNA) is designed for 5GHz wireless LAN systems based on IEEE802.11a and HiperLAN2 standards. The MAX2649 achieves a 2.1dB noise figure, 17dB gain, and 0dBm IIP3, making it ideal as a first-stage LNA in 5GHz OFDM WLAN radio systems.

This device operates over a +2.7V to +3.6V supply range and features low overall current consumption (12.5mA). The MAX2649 also includes a shutdown mode to save power when the receiver is inactive.

The LNA is designed on a low-noise, advanced SiGe process optimized for high-frequency applications. The device is available in a tiny 2 × 3 chip-scale package (UCSP™) (1mm × 1.5mm).

Applications

IEEE802.11a Wireless LAN

ETSI HiperLAN2 WLAN

5GHz ISM Radios

5GHz Cordless Phones

Features

- ♦ **4.9GHz to 5.9GHz Wideband Operation**
- ♦ **Low-Noise Figure: 2.1dB**
- ♦ **High Gain: 17dB**
- ♦ **High IIP3: 0dBm**
- ♦ **Shutdown Mode**
- ♦ **+2.7V to +3.6V Single-Supply Operation**
- ♦ **1mm × 1.5mm UCSP**

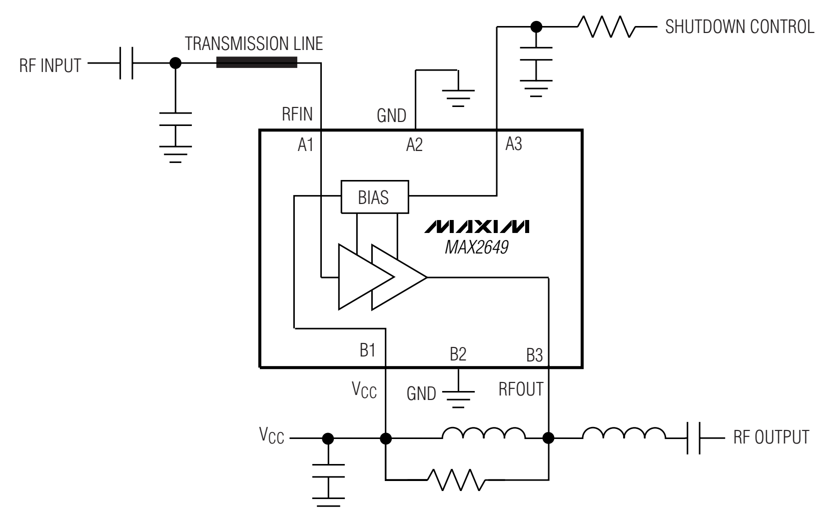
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2649EBT-T	-40°C to +85°C	2 x 3 UCSP*

**Requires special solder temperature profile described in the Absolute Maximum Ratings section.*

Pin Configuration appears at end of data sheet.

Functional Diagram/Typical Operating Circuit



FOR LAYOUT AND DESIGN DETAILS, PLEASE REFER TO THE MAX2649 EV KIT.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +4.2V
$\overline{SHDN}$ to GND...-0.3V to (V_{CC} + 0.3V)
RFIN to GND..-0.3V to +0.9V
RFOUT to GND..-0.3V to (V_{CC} + 0.3V)
RF Input Power (50Ω Source) ....+5dBm
Continuous Power Dissipation (T_A = +70°C)
2 x 3 UCSP (derate 24mW/°C above +70°C) 500mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Bump Temperature (soldering) (Note 1)
Infrared (15s) ....+220°C
Vapor Phase (60s) ....+215°C

Note 1: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits the use of only the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not recommended.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, no RF signal applied, V_{IH} = +2.0V, V_{IL} = +0.4V, RFIN and RFOUT terminated to 50Ω through DC-blocking caps, T_A = -40°C to +85°C. Typical values are at +3.0V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.7		3.6	V
Active Supply Current	I_{CC}			12.5	20	mA
Shutdown Supply Current	I_{CC}	$\overline{SHDN}$ = V_{IL}		0.3	10	µA
Digital Input Logic High	V_{IH}		2			V
Digital Input Logic Low	V_{IL}				0.4	V
Digital Input Current					5	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2649 EV kit, V_{CC} = +3.0V, P_{IN} = -30dBm, RFIN and RFOUT terminated to 50Ω through DC-blocking caps, V_{IH} = +2.0V, V_{IL} = +0.4V, T_A = +25°C. Typical values are at f_{RF} = 5250MHz, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Note 4)	4900		5900	MHz
Power Gain	$\|S_{21}\|$	f_{RF} = 5150MHz to 5350MHz (Note 5)	15	17		dB
Gain Variation Over Temperature				0.2	1.5	dB
Noise Figure	NF	f_{RF} = 5150MHz to 5350MHz (Note 6)		2.1	2.5	dB
Input Third-Order Intercept Point	IIP3	Two tones at 5250MHz and 5251MHz, -30dBm per tone (Note 6)	-3.5	0		dBm
Input Return Loss	$\|S_{11}\|$			-12		dB
Output Return Loss	$\|S_{22}\|$			-16		dB
Reverse Isolation	$\|S_{12}\|$			-30		dB
Turn-On Time	t_{ON}			0.3	0.8	µs
Turn-Off Time	t_{OFF}			0.5	1.2	µs

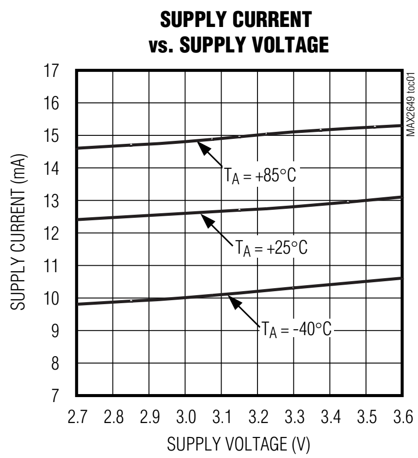
AC ELECTRICAL CHARACTERISTICS (continued)

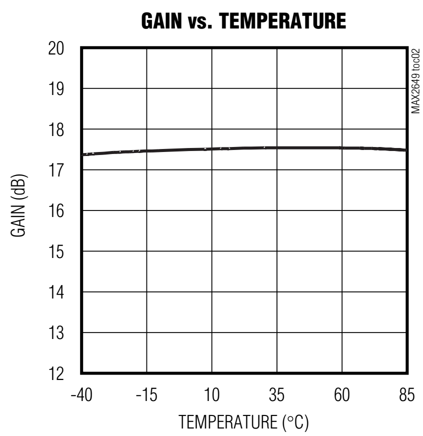
(MAX2649 EV kit, V_{CC} = +3.0V, P_{IN} = -30dBm, RFIN and RFOUT terminated to 50Ω through DC-blocking caps, V_{IH} = +2.0V, V_{IL} = +0.4V, T_A = +25°C. Typical values are at f_{RF} = 5250MHz, unless otherwise noted.) (Note 3)

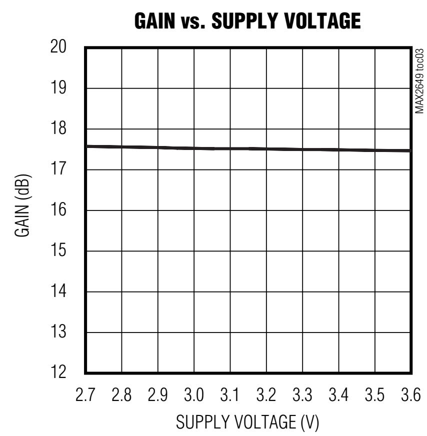
Note 2: DC characteristics are production tested at T_A = +85°C. DC specifications over temperature are guaranteed by design and characterization.
Note 3: Specifications are guaranteed by design and characterization.
Note 4: Recommended band of operation.
Note 5: Specifications are corrected for board losses on the MAX2649 EV kit (0.5dB at input, 0.5dB at output).
Note 6: Specifications are corrected for board losses on the MAX2649 EV kit (0.5dB at input).

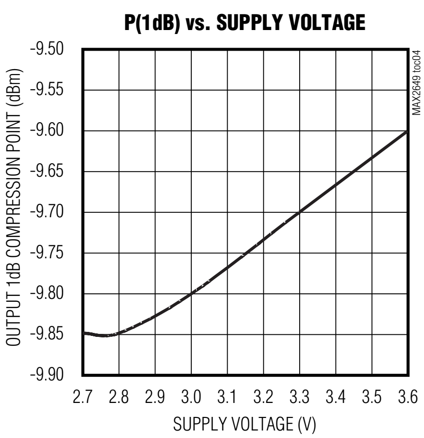
Typical Operating Characteristics

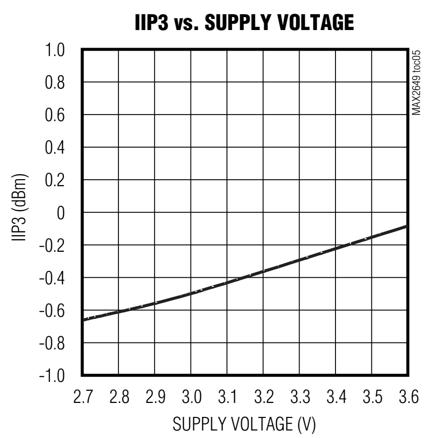
(Data taken on board optimized for f_{RF} = 5150MHz to 5350MHz.) (V_{CC} = +3.0V, f_{RF} = 5250MHz, P_{IN} = -30dBm, and T_A = +25°C, unless otherwise noted.)

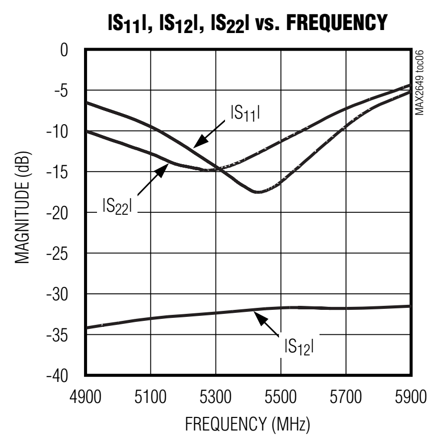






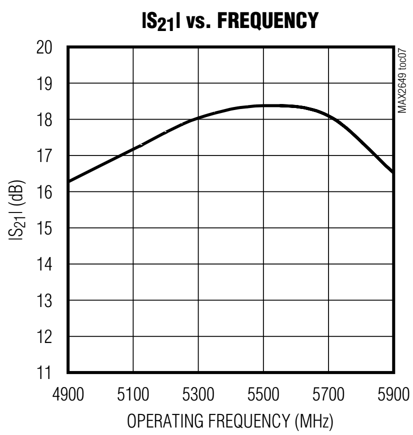


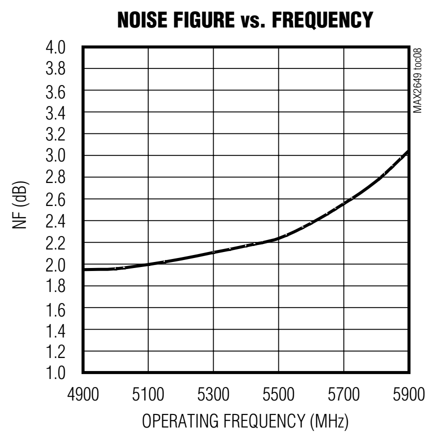


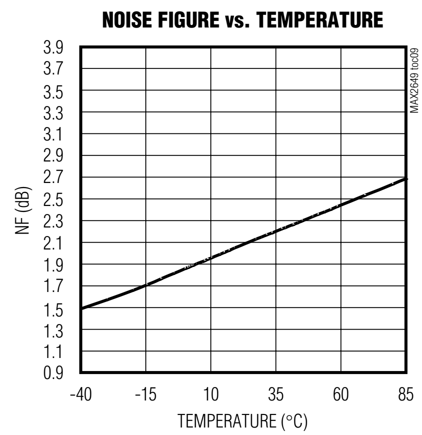


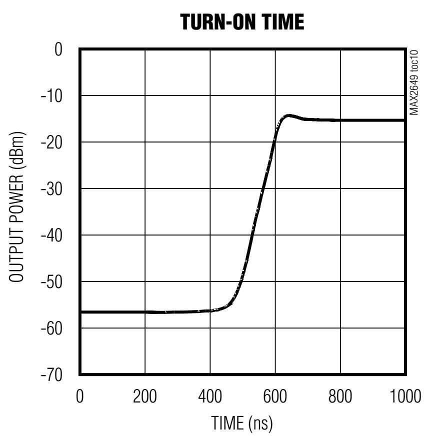
Typical Operating Characteristics (continued)

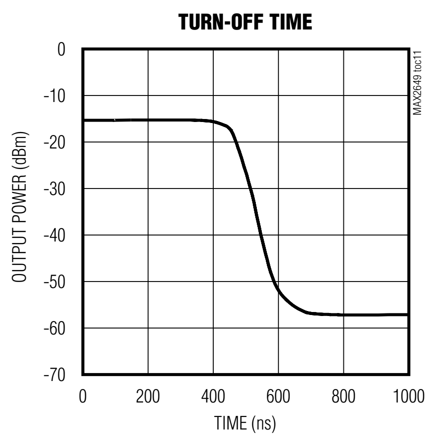
(Data taken on board optimized for f_{RF} = 5150MHz to 5350MHz.) (V_{CC} = +3.0V, f_{RF} = 5250MHz, P_{IN} = -30dBm, and T_A = +25°C, unless otherwise noted.)











Pin Description

PIN	NAME	FUNCTION
A1	RFIN	LNA Input. Requires shunt capacitor and transmission line for input matching. (See the *Typical Operating Circuit* and refer to the MAX2649 EV kit data sheet for details.)
A2, B2	GND	Ground. For optimum performance, provide a low-inductance connection to the ground plane.
A3	$\overline{SHDN}$	Shutdown. Apply logic signal through 100Ω resistor with a 20pF shunt capacitor to ground. Set $\overline{SHDN}$ high for active operation. Set $\overline{SHDN}$ low to place the part in shutdown mode.
B1	V_{CC}	+2.7V to +3.6V Supply Pin. Bypass with 100pF capacitor. (See the *Typical Operating Circuit* and refer to the MAX2649 EV kit data sheet for details.)
B3	RFOUT	LNA Output. Requires external matching network for optimal performance. (See the *Typical Operating Circuit* and refer to the MAX2649 EV kit data sheet for details.)

Detailed Description

The MAX2649 LNA operates with RF frequencies of 4.9GHz to 5.9GHz. This device is ideal for IEEE802.11a and HiperLAN2 applications. This device is available in a 6-bump UCSP package and contains internal bias circuitry and shutdown circuitry to minimize the number of required external components.

Applications Information

Optimal gain and noise-figure performance require input- and output-matching circuits tuned for the band of interest. All electrical specifications and typical operating characteristics are measured on the MAX2649 evaluation kit (EV kit), which is tuned for operation in the 5.15GHz to 5.35GHz band. Referencing the application circuit, PC board layout, and components specified in the MAX2649 EV kit data sheet reduces evaluation and design time for five system designs. For applications in other bands, refer to the MAX2649 S-parameters, noise parameters, and the following comments to aid design. The S-parameters and noise parameters are available at www.maxim-ic.com.

Input Matching

The input stage is internally biased, so no external bias circuitry is required at RFIN. Be sure to AC-couple to the input. Because the noise figure of the LNA design is severely degraded by low-Q matching components, always design with high-Q wire-wound inductors and low-loss capacitors. Remember that package parasitics must be taken into consideration; always use components with self-resonant frequencies higher than the intended frequency of operation.

Output Matching

The output of the MAX2649 is an open-collector transistor; the DC bias and RF matching network are off-chip, as illustrated in the *Typical Operating Circuit*. Bias the output stage with V_{CC} through an RF choke. The collector is in series with a small inductor and then AC-coupled to the RF output. If necessary, place a shunt capacitor to ground at the far end of the inductor to provide better matching. S-parameters and noise parameters can be found at www.maxim-ic.com.

Power-Supply Bypassing

Proper power-supply bypassing is essential for high-frequency circuit stability. Place a small-value capacitor as close to the IC as possible to decouple high-frequency noise. Place a larger-value capacitor near the supply to decouple low-frequency noise. Whenever possible, place the ground-connected side of bypass capacitors within a few millimeters of the IC's ground connections.

Layout information

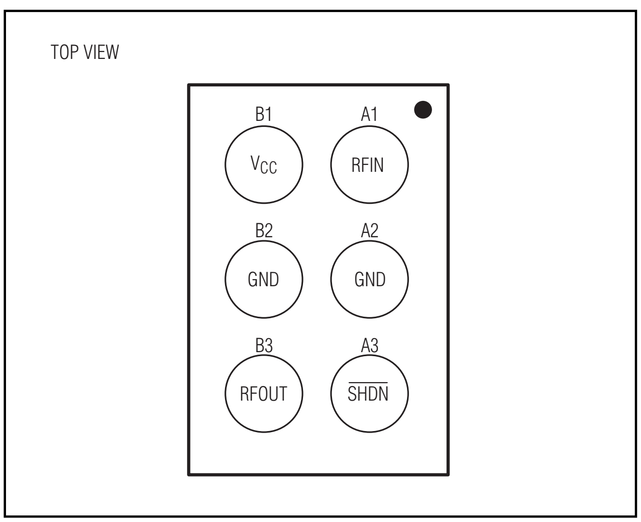
A properly designed PC board is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, EMI, and stray inductance. Use multiple, separate low-inductance-plated vias to the ground plane for each ground bump.

The chip-scale package (UCSP) has a bump pitch of 0.5mm (19.7mil) and a bump diameter of 0.3mm (12mil). Therefore, lay out the solder pad spacing on 0.5mm (19.7mil) centers, and use a pad size of 0.25mm (10mil), and a solder mask opening of 0.33mm (13mil). Round or square pads are permissible. Refer to the Maxim application note, *Wafer Level Chip-Scale Packaging*, for additional detailed information on UCSP layout and handling.

UCSP Reliability

The chip-scale package (UCSP) represents a unique package that greatly reduces board space compared to other packages. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. Operating life test and moisture resistance remains uncompromised, as it is primarily determined by the wafer-fabrication process. Mechanical stress performance is a greater consideration for a UCSP. UCSP solder-joint contact integrity must be considered because the package is attached through direct solder contact to the user's PC board. Testing done to characterize the UCSP reliability performance shows that it is capable of performing reliably through environmental stresses. Results of environmental stress tests and additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website, www.maxim-ic.com/1st_pages/UCSP.htm.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 471

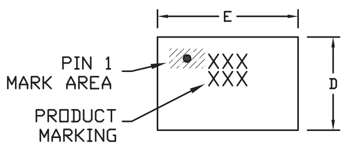
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6L, UCSP.EPS

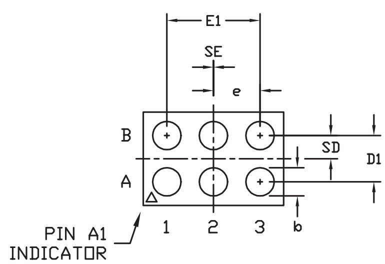
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	0.50 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B6-1	1.00±0.05	1.52±0.05	NONE
B6-2	1.00±0.05	1.52±0.05	B2
B6-3	1.05±0.05	1.57±0.05	NONE
B6-4	1.05±0.05	1.57±0.05	B2
B6-5	0.97±0.05	1.46±0.05	NONE
B6-6	1.16±0.05	1.57±0.05	NONE

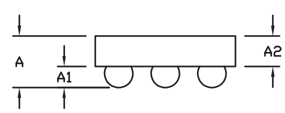


TOP VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 3x2 UCSP
APPROVAL | DOCUMENT CONTROL NO. 21-0097 | REV. G | 1/1